Lab 4A
(Full Score: 100 points)

(**Due by 4/14/Thursday at at Moodle**)

Your name:	Score:

Design and Implementation of an 4-bit ALU (Arithmetic and Logic Unit)

Goal

- To design and implement an 4-bit ALU.
- To design and implement the logic circuits for generating 4 status bits, Z, N, V, C.
- To learn how to work as a team to work on a project

Objectives

- To design a 4-bit ALU module based on a set of given requirements
- To implement the 4-bit ALU design using Altera's Quartus II CAD software, including design entry, compilation, simulation and download to DE2 board

Detailed Requirements

I. Building a 4-bit ALU module based on the circuit on the slide 20 of ALU Lecture at http://www.cs.uiuc.edu/class/fa05/cs231/lectures/11-ALU.ppt

- You must start from the first slide of the Lecture
- The circuit there does NOT have circuits for Z, N, V, C outputs, so you must inserts circuits for them.
- $X = X_3X_2X_1X_0$ and $Y = Y_3Y_2Y_1Y_0$ are two 4-bit signed numbers (for arithmetic operations) or unsigned numbers (for logic operations) to the inputs of the ALU
- The outputs of the ALU are: $G = G_3G_2G_1G_0$
- The ALU has 4 status outputs: N, V, Z, C defined as:
  N = 0/1 – Non-Negative Result/Negative Result
  V = 0/1 – No Overflow/Overflow
  Z = 0/1 – Non-Zero/Zero
  C = 0/1 – Carry of 0 /Carry of 1

- You **must use the following PIN assignment** table for the inputs and outputs of your circuits. I'll use this table to test your circuit. If you ***don't use*** this table in the PIN assignments in your circuit, your implementation will ***have NO chance*** to pass the testing even though you have correctly designed/implemented the project, which means a ***huge deduction*** of your credits!

INPUTS	X_3	**SW[11],PIN_P1**
	X_2	**SW[10],PIN_N1**
	X_1	**SW[9],PIN_A13**
	X_0	**SW[8],PIN_B13**
	Y_3	**SW[7],PIN_C13**
	Y_2	**SW[6],PIN_AC13**
	Y_1	**SW[5],PIN_AD13**
	Y_0	**SW[4],PIN_AF14**
	S_3	**SW[3],PIN_AE14**
	S_2	**SW[2],PIN_P25**
	S_1	**SW[1],PIN_N26**
	S_0	**SW[0],PIN_N25**
OUTPUTS	G_3	**LEDG[7],PIN_Y18**
	G_2	**LEDG[6],PIN_AA20**
	G_1	**LEDG[5],PIN_U17**
	G_0	**LEDG[4],PIN_U18**
	Z	**LEDG[3],PIN_V18**
	N	**LEDG[2],PIN_W19**
	V	**LEDG[1],PIN_AF22**
	C	**LEDG[0],PIN_AE22**

II. Test the 4-bit ALU Module

Perform a complete functional simulation of your 4-bit ALU module. To do so, you must develop a simulation plan that should cover as many typical cases and as many special cases as possible. Using the following table to test your implementation (you may need to design more test cases).

ALU Control				X input				Y input				ALU output				Status Bits			
S_3,	S_2,	S_1,	S_0	X_3,	X_2,	X_1,	X_0	Y_3,	Y_2,	Y_1,	Y_0	G_3,	G_2,	G_1,	G_0	N	V	Z	C
0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	0	0	0	0
1	x	1	1	0	0	1	1	1	0	0	0	1	1	0	0	1	0	0	0
1	x	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	1	0
1	x	1	0	0	0	1	1	1	0	0	0	1	0	1	1	1	0	0	0
0	0	0	1	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	0	0	0	1	1	1	0	0	0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	1	1	1	0	0	0	1	0	1	1	1	0	0	0
0	1	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0
0	0	0	0	1	1	0	1	0	1	1	1	1	1	0	1	1	0	0	0
1	x	0	1	1	0	0	1	0	0	0	1	1	0	0	1	1	0	0	0
1	x	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	1	0
1	x	1	0	0	1	1	1	0	1	1	1	0	0	0	0	0	0	1	0
0	0	0	1	1	1	1	1	0	1	1	1	0	0	0	0	0	0	1	1
0	1	1	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	1	1
0	0	1	0	0	1	0	1	0	1	1	1	1	1	0	0	1	1	0	0
0	1	0	1	1	1	0	1	0	1	1	1	0	1	1	0	0	1	0	1

This is a **group project**. A team of **2 members** work together and only one submission is required!

- **But** if you have completed the lab **individually**, you will receive ***up to 15%*** extra points.

Submissions:

- Your COMPLETE QuartusII project (compresses in a zip file).
- (Submitted to Moodle by the due time).