Assignment 4
(Full Score: 100 points)
(Due in class, **4/20/Wednesday**,)

Your name:	Score:

1. The following memories are specified by the number of words times the number of bits per word. How many address lines and input– output data lines are needed in each case?

(a) 48K × 8,
(b) 512K × 32,
(c) 64M × 64, and
(d) 2G × 1.

2. Word number $(835)_{10}$ in the memory shown in the following figure contains the binary equivalent of $(15{,}103)_{10}$. List the 10-bit address and the 16-bit memory contents of the word.

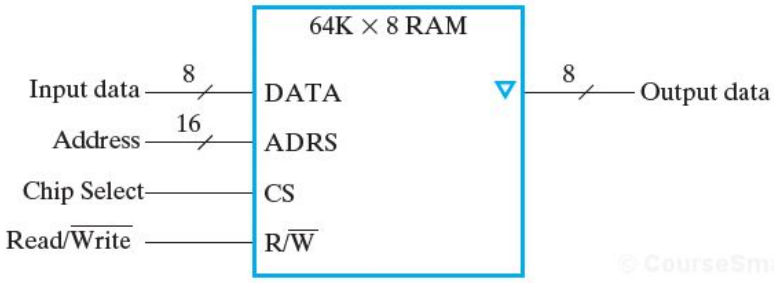
Memory Address		
Binary	Decimal	Memory Contents
0000000000	0	10110101 01011100
0000000001	1	10101011 10001001
0000000010	2	00001101 01000110
	.	.
	.	.
	.	.
	.	.
	.	.
1111111101	1021	10011101 00010101
1111111110	1022	00001101 00011110
1111111111	1023	11011110 00100100

Contents of a 1024 × 16 Memory

3. (a) How many 128K × 16 RAM chips are needed to provide a memory capacity of 2 MB?
(b) How many address lines are required to access 2 MB? How many of these lines are connected to the address inputs of all chips?
c) How many lines must be decoded to produce the chip select inputs? Specify the size of the decoder.

4. Explain how a DDRAM achieves a data rate that is a factor of two higher than a comparable SDRAM.

5. Using the 64K × 8 RAM chip in the following figure plus a decoder, construct the block diagrams for (a) a **512K x 8 RAM**, and (b) a **256K × 16 RAM**.



Symbol for a 64K × 8 RAM Chip

6. Given the following Truth Table, design and implement it with (a) a decoder and OR gates (as shown in the slides "ROM examples, you may use "abbreviated OR" gates), and (b) PLA.

Address $A_2A_1A_0$	Data $V_2V_1V_0$
000	001
001	101
010	110
011	100
100	101
101	001
110	011
111	000